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A description is given of the Kinden environment, which combines object-oriented modeling and model-based reasoning to capture, integrate, and manage VLSI design process attributes and hierarchies.

### **Hierarchical Modeling of the VLSI Design Process**

Test generation is one of the most difficult tasks facing the designer of complex VLSI-based digital systems. Much of this difficulty is attributable to the almost universal use in testing of low, gate-level circuit and fault models that predate integrated circuit technology.

### **Hierarchical Modeling For Vlsi Circuit Testing, Debashis**

Hierarchical modeling of the VLSI design process Abstract: A description is given of the Kinden environment, which combines object-oriented modeling and model-based reasoning to capture, integrate, and manage VLSI design process attributes and hierarchies.

### **Hierarchical modeling of the VLSI design process - IEEE**

Chapter 8 Hierarchical Models In the (generalized) linear models weâ€™ve looked at so far, weâ€™ve assumed that the observations are independent of each other given the predictor variables.

### **Chapter 8 Hierarchical Models - Division of Social Sciences**

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